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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/609,384	KODATE ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-11 and 13-16* is/are pending in the application.

4a) Of the above claim(s) *8,11 and 14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,9,10,13,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 October 2008 has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings were received on 21 October 2008. These drawings are acceptable.

4. The drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the figures.

Specification

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 2-7, 9, 10, 13, 15, and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***an electric field produced by the first data line***" (in line 7) and "***an electric field produced by the first data line***" (in line 9).

It would be unclear to one having ordinary skill in the art what, if any, structural and/or operational relationship exists between each of the "***electric field***" limitations. For example:

Is a single, identical "***electric field***" being claimed? Or are distinct, different, and independent "***electric fields***" being claimed?

9. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a first conductive layer***" (in line 3); "***a first lower layer***" (in line 4).

It would be unclear to one having ordinary skill in the art what, if any, structural and/or operational relationship exists between each of the "***layer***" limitations. For example:

Is a single, identical "***layer***" being claimed? Or are distinct, different, and independent "***layers***" being claimed?

An omitted structural cooperative relationship results from the claimed subject matter: "***a second conductive layer***" (in line 5); "***a second lower layer***" (in line 6).

It would be unclear to one having ordinary skill in the art what, if any, structural and/or operational relationship exists between each of the "***layer***" limitations. For example:

Is a single, identical "***layer***" being claimed? Or are distinct, different, and independent "***layers***" being claimed?

10. Claim 9 recites the limitation "***a second potential***" (line 4). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill in the art whether or not a "***a first potential***" is intended to claimed.

11. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***an electric field produced by the first data line***" (in line 8) and "***an electric field produced by the first data line***" (in line 10).

It would be unclear to one having ordinary skill in the art what, if any, structural and/or operational relationship exists between each of the "***electric field***" limitations. For example:

Is a single, identical "***electric field***" being claimed? Or are distinct, different, and independent "***electric fields***" being claimed?

12. Claim 15 recites the limitation "***a second potential***" (line 3). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill in the art whether or not a "***a first potential***" is intended to claimed.

13. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

14. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 102 / 103

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

18. Claims 2-7, 9, 10, 13, 15, and 16 are rejected under 35 U.S.C. 102(b) as anticipated by ***Sakamoto (US 6,028,577 A)***; or, in the alternative, under 35 U.S.C. 103(a) as obvious over ***Sakamoto (US 6,028,577 A)*** in view of the ***Instant Application's Admitted Prior Art (AAPA)***.

Regarding claim 2, ***Sakamoto*** discloses an image display element [*e.g., Figs. 7 & 10A*] comprising:

a plurality of data lines [*e.g., Figs. 7 & 10A; 3*] including a first data line [*e.g., Figs. 7 & 10A; 3(j)*];

a plurality of scan lines [*e.g., Figs. 7 & 10A; 2*] including a first scan line [*e.g., Figs. 7 & 10A; 2(i)*] and a second scan line [*e.g., Figs. 7 & 10A; 2(i+1)*];

a first pixel electrode [*e.g., Figs. 7 & 10A; 1(i, j)*] and a second pixel electrode [*e.g., Figs. 7 & 10A; 1(i+1, j)*] that are electrically connected to the first data line (*see the entire document, including Column 11, Lines 35-61*);

a first electrostatic shielding unit [*e.g., Fig. 7; 7a (left side)*] that shields the first pixel electrode from an electric field produced by the first data line;

a second electrostatic shielding unit [*e.g., Fig. 7; 7a (right side)*] that shields the second pixel electrode from an electric field produced by the first data line (*see the entire document, including Column 13, Lines 17-52*);

a first switching device [*e.g., Fig. 10B; 6(i, j)*] having a first gate electrode, a first source electrode and a first drain electrode, wherein

the first source electrode is electrically connected to the first data line and

the first drain electrode is electrically connected to the first pixel electrode;

a second switching device [*e.g., Fig. 10B; 6(i, j-1), 6(i+1, j-1)*] having a second gate electrode, a second source electrode and a second drain electrode, wherein

the second drain electrode is electrically connected to the first gate electrode,

the second source electrode is electrically connected to the first scan line and

the second gate electrode is electrically connected to the second scan line; and

a third switching device [*e.g., Fig. 10B; 6(i+1, j)*] having a third gate electrode, a third source electrode and a third drain electrode, wherein

the third source electrode is electrically connected to the first data line,

the third drain electrode is electrically connected to the second pixel electrode and

the third gate electrode is electrically connected to the first scan line (*see the entire document, including Column 11, Line 62 - Column 12, Line 67*).

One having ordinary skill in the art at the time of invention would have recognized that ***Sakamoto's*** switching devices are "*electrically connected*" as instantly claimed, because ***Sakamoto's*** switching devices are all linked together in a single LCD electrical circuit.

However, should it be shown that ***Sakamoto*** teaches such "*switching device electrical connections*" with insufficient specificity:

The ***AAPA*** discloses an image display element [*e.g., Fig. 14*] comprising:

a plurality of data lines [*e.g., Fig. 14; D*] including a first data line [*e.g., Fig. 14;* D_m];

a plurality of scan lines [*e.g., Fig. 14; G*] including a first scan line [*e.g., Fig. 14;* G_{n+2}] and a second scan line [*e.g., Fig. 14;* G_{n+1}];

a first pixel electrode [*e.g., Fig. 14;* A_1] and a second pixel electrode [*e.g., Fig. 14;* B_1] that are electrically connected to the first data line;

a first switching device [*e.g., Fig. 14;* M_1] having a first gate electrode, a first source electrode and a first drain electrode, wherein

the first source electrode is electrically connected to the first data line and

the first drain electrode is electrically connected to the first pixel electrode;

a second switching device [*e.g., Fig. 14;* M_2] having a second gate electrode, a second source electrode and a second drain electrode, wherein

the second drain electrode is electrically connected to the first gate electrode,

the second source electrode is electrically connected to the first scan line and

the second gate electrode is electrically connected to the second scan line; and

a third switching device [*e.g., Fig. 14;* M_3] having a third gate electrode, a third source electrode and a third drain electrode, wherein

the third source electrode is electrically connected to the first data line,

the third drain electrode is electrically connected to the second pixel electrode and

the third gate electrode is electrically connected to the first scan line (*see the entire* **AAPA**, *including Pages 1-4*).

Sakamoto and the ***AAPA*** are analogous art, because they are from the shared inventive field of active matrix liquid crystal display devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to apply ***Sakamoto's*** a first and second electrostatic shielding units to the ***AAPA's*** multiplexed image structure, so as to prevent brightness unevenness improve image quality [*e.g.,* ***Sakamoto****: Column 8, Lines 1-61*] while requiring a lesser number of data lines driving integrated circuits, it becomes possible to lower the manufacturing cost and improve the productivity [*e.g.,* ***AAPA****: Page 2, Lines 19-21*].

Regarding claim 3, ***Sakamoto*** discloses the first electrostatic shielding unit is formed by a first conductive layer [*e.g., Fig. 8; 7a (left side)*] that is disposed adjacent to the first data line in a first lower layer than the first pixel electrode [*e.g., Fig. 8; 1(i, j)*], and

the second electrostatic shielding unit is formed by a second conductive layer [*e.g., Fig. 8; 7a (right side)*] that is disposed adjacent to the first data line in a second lower layer than the second pixel electrode [*e.g., Fig. 8; 1(i+1, j)*] (*see the entire document, including Column 13, Lines 55-59*).

Regarding claim 4, ***Sakamoto*** discloses the first electrostatic shielding unit [*e.g., Fig. 8; 7a (left side)*] and the first pixel electrode [*e.g., Fig. 8; 1(i, j)*] have areas that are partially superimposed with each other in a layer direction of the first pixel electrode, and

the second electrostatic shielding unit [*e.g., Fig. 8; 7a (right side)*] and the second pixel electrode[*e.g., Fig. 8; 1(i+1, j)*] have areas that are partially superimposed with each other in a layer direction of the second pixel electrode (*see the entire document, including Column 13, Lines 55-59*).

Regarding claim 5, ***Sakamoto*** discloses a first capacitor line [*e.g., Figs. 7 & 10B; C2*] that is disposed in an area partially superimposed with the first pixel electrode in the layer direction of the first pixel electrode, and

that is connected to the first electrostatic shielding unit; and

a second capacitor line [*e.g., Figs. 7 & 10B; C1*] that is disposed in an area partially superimposed with the second pixel electrode in the layer direction of the second pixel electrode, and

that is connected to the second electrostatic shielding unit (*see the entire document, including Column 13, Line 65 - Column 14, Line 6*).

Regarding claim 6, ***Sakamoto*** discloses the first electrostatic shielding unit and the second electrostatic shielding unit are electrically connected to each other (*see the entire document, including Fig. 7; Column 13, Lines 17-28*).

Regarding claim 7, ***Sakamoto*** discloses the first electrostatic shielding unit and the second electrostatic shielding unit are electrically connected to a wiring structure that has a first potential (*see the entire document, including Fig. 7; Column 13, Lines 17-59*).

Regarding claim 9, ***Sakamoto*** discloses the first electrostatic shielding unit and the second electrostatic shielding unit are connected to a potential supply line that has a second potential (*see the entire document, including Fig. 7; Column 13, Lines 17-59*).

Regarding claim 10, ***Sakamoto*** discloses the second potential is maintained within a range of a potential variation of the first and second pixel electrodes (*see the entire document, including Fig. 7; Column 13, Lines 17-59*).

Regarding claim 13, ***Sakamoto*** discloses an image display device [*e.g., Figs. 7 & 10A*] comprising:

a data line driving circuit [*e.g., Fig. 10A; 5*] that supplies a display signal to a first data line [*e.g., Figs. 7 & 10A; 3(j)*];

a scan line driving circuit [*e.g., Fig. 10; 4*] that supplies a scan signal to a first scan line [*e.g., Figs. 7 & 10A; 2(i)*] and a second scan line [*e.g., Figs. 7 & 10A; 2(i+1)*];

a first pixel electrode [*e.g., Figs. 7 & 10A; 1(i, j)*] and a second pixel electrode [*e.g., Figs. 7 & 10A; 1(i+1, j)*] that are supplied with the display signal from the first data line (*see the entire document, including Column 11, Lines 35-61*);

a first electrostatic shielding unit [*e.g., Fig. 7; 7a (left side)*] that shields the first pixel electrode from an electric field produced by the first data line;

a second electrostatic shielding unit [*e.g., Fig. 7; 7a (right side)*] that shields the second pixel electrode from an electric field produced by the first data line (*see the entire document, including Column 13, Lines 17-52*);

a first switching device [*e.g., Fig. 10B; 6(i, j)*] having a first gate electrode, a first source electrode and a first drain electrode, wherein

the first source electrode is electrically connected to the first data line and

the first drain electrode is electrically connected to the first pixel electrode;

a second switching device [*e.g., Fig. 10B; 6(i, j-1), 6(i+1, j-1)*] having a second gate electrode, a second source electrode and a second drain electrode, wherein

the second drain electrode is electrically connected to the first gate electrode,

the second source electrode is electrically connected to the first scan line and

the second gate electrode is electrically connected to the second scan line; and

a third switching device [*e.g., Fig. 10B; 6(i+1, j)*] having a third gate electrode, a third source electrode and a third drain electrode, wherein

the third source electrode is electrically connected to the first data line,

the third drain electrode is electrically connected to the second pixel electrode and

the third gate electrode is electrically connected to the first scan line (*see the entire document, including Column 11, Line 62 - Column 12, Line 67*).

One having ordinary skill in the art at the time of invention would have recognized that ***Sakamoto's*** switching devices are "*electrically connected*" as instantly claimed, because ***Sakamoto's*** switching devices are all linked together in a single LCD electrical circuit.

However, should it be shown that ***Sakamoto*** teaches such "*switching device electrical connections*" with insufficient specificity:

The ***AAPA*** discloses an image display device [*e.g., Fig. 14*] comprising:

a data line driving circuit that supplies a display signal to a first data line [*e.g., Fig. 14; D_m*];

a scan line driving circuit that supplies a scan signal to a first scan line [*e.g., Fig. 14; G_{n+2}*] and a second scan line [*e.g., Fig. 14; G_{n+1}*];

a first pixel electrode [*e.g., Fig. 14; A_1*] and a second pixel electrode [*e.g., Fig. 14; B_1*] that are supplied with the display signal from the first data line;

a first switching device [*e.g., Fig. 14; M_1*] having a first gate electrode, a first source electrode and a first drain electrode, wherein

the first source electrode is electrically connected to the first data line and

the first drain electrode is electrically connected to the first pixel electrode;

a second switching device [*e.g., Fig. 14; M_2*] having a second gate electrode, a second source electrode and a second drain electrode, wherein

the second drain electrode is electrically connected to the first gate electrode,

the second source electrode is electrically connected to the first scan line and

the second gate electrode is electrically connected to the second scan line; and

a third switching device [*e.g., Fig. 14; M_3*] having a third gate electrode, a third source electrode and a third drain electrode, wherein

the third source electrode is electrically connected to the first data line,

the third drain electrode is electrically connected to the second pixel electrode and

the third gate electrode is electrically connected to the first scan line (*see the entire* **AAPA**, *including Pages 1-4*).

Sakamoto and the ***AAPA*** are analogous art, because they are from the shared inventive field of active matrix liquid crystal display devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to apply ***Sakamoto's*** a first and second electrostatic shielding units to the ***AAPA's*** multiplexed image structure, so as to prevent brightness unevenness improve image quality [*e.g., **Sakamoto**: Column 8, Lines 1-61*] while requiring a lesser number of data lines driving integrated circuits, it becomes possible to lower the manufacturing cost and improve the productivity [*e.g., **AAPA**: Page 2, Lines 19-21*].

Regarding claim 15, ***Sakamoto*** discloses the first electrostatic shielding unit and the second electrostatic shielding unit are connected to a potential supply line that has a second potential (*see the entire document, including Fig. 7; Column 13, Lines 17-59*).

Regarding claim 16, ***Sakamoto*** discloses the second potential is maintained within a range of a potential variation of the first pixel electrode (*see the entire document, including Fig. 7; Column 13, Lines 17-59*).

Response to Arguments

19. Applicant's arguments filed 21 October 2008 have been fully considered but they are not persuasive.

The Applicant contends, "*With respect to presently pending independent claim 2, Sakamoto did not disclose or suggest that "the second drain electrode (of the second switching device) is electrically connected to the first gate electrode (of the first switching device)", as recited in claim 2. Rather, Sakamoto discloses that the drain electrode of the second switching device (see Figure 10B; 6(i, j-l)) is electrically connected to a third pixel electrode (see Fig. 10B; 1 (i, j- 1)).*

Still further, Sakamoto also did not disclose or suggest that "the second source electrode (of the second switching device) is electrically connected to the first scan line", as recited in claim 2. Rather, Sakamoto discloses that the source electrode of the second switching device (see Fig. 10B; 6(i, j-l)) is electrically connected to a second data line (see Fig. 10B; 30-1)).

Also, Sakamoto does not disclose or suggest that "the second gate electrode (of the second switching device) is electrically connected to the second scan line", as recited in claim 2. Rather, Sakamoto discloses that the gate electrode of the second switching device (see Fig. 10B;

60, j-l)) is electrically connected to the first scan line (see Fig. 10B; 2(i))" (see Pages 10-11 of the Response filed 21 October 2008). However, the examiner respectfully disagrees.

One having ordinary skill in the art at the time of invention would have recognized that ***Sakamoto's*** switching devices are "*electrically connected*" as instantly claimed, because ***Sakamoto's*** switching devices are all linked together in a single LCD electrical circuit.

Applicant's arguments with respect to claims 2-7, 9, 10, 13, 15, and 16 have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571)272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
29 January 2009